AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (withdrawn) A data processor having an SIMD type execution unit:

said data processor having an instruction to cause said SIMD type execution unit to process vector data.

2. (withdrawn) A data processor, as claimed in Claim 1, wherein:

said SIMD type execution unit has a plurality of execution units for performing multiply-add operations on floating-point numbers.

3. (withdrawn) A data processor for executing instructions in an instruction set and having an SIMD type execution unit, wherein:

said instruction set includes an instruction for causing said SIMD type execution unit to operate on vector data.

4. (withdrawn) A data processor, as claimed in Claim 3, wherein:

said SIMD type execution unit has a plurality of execution units for performing multiply-add operations on floating-point numbers.

5. (currently amended) A data processor for executing instructions in an instruction set, wherein:

said instruction set includes an instruction for causing said data processor to calculate an inner product of two vectors and to sum said inner product with scalar data, with a single execution of said instruction. ~~the sum of the inner product of vectors and scalar data.~~

6. (currently amended) A data processor~~, as claimed in~~ according to Claim 5[[:]], wherein:

said data processor ~~having~~ includes a floating-point execution unit for calculating the inner product of a length-4 vector and another length-4 vector and ~~the sum of~~summing said inner product and scalar data.

7. (currently amended) A data processor~~, as claimed in~~ according to Claim 6, wherein:

said floating-point execution unit ~~has~~ includes a 9 input adder.

8. (currently amended) A data processor for executing instructions in an instruction set, wherein:

said instruction set includes an instruction for causing said data processor to calculate ~~the~~ a product of matrix data and vector data, with a single execution of said instruction.

9. (currently amended) A data processor~~, as claimed in~~ according to Claim 8[[:]], wherein:

said data processor ~~having~~ includes a plurality of floating-point execution units for calculating ~~the~~ an inner product of a vector and another vector.

10. (currently amended) A data processor~~, as claimed in~~ according to Claim 8, wherein:

said matrix data are 4 × 4 matrix data and said vector data are length-4 vectors.

11. (currently amended) A data processor~~, as claimed in~~ according to Claim 9, wherein:

each of said plurality of floating-point execution units is an execution unit capable of calculating ~~the~~ a sum of ~~said~~ inner product and scalar data.

12. (currently amended) A data ~~processing system, as claimed in~~processor according to Claim 11, wherein:

said execution unit ~~has~~ includes a 9-input adder.